AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application;

--1. (Currently Amended) A semiconductor apparatus having a delay monitor circuit for ~~perceiving~~ monitoring critical path delay characteristics of a target circuit, wherein[[:]] said delay monitor circuit comprises:

[[a]] delay means having a plurality of delay elements for forming delay element arrays in accordance with supplied configuration information including a delay component to cause a signal propagation delay ~~inside~~ in said target circuit;

a plurality of registers ~~to be set~~ for setting therein a plurality of configuration ~~information~~ informations for forming said delay element arrays; and

[[a]] switching means for selectively switching the configuration information of said plurality of registers and supplying the configuration information to said delay means.

--2. (Currently Amended) [[A]] The semiconductor apparatus as set forth in claim 1, wherein said switching means switches the configuration information of the delay element arrays set in the plurality of registers in a time sharing ~~way~~ manner and supplies the configuration information to said delay means.

--3. (Currently Amended) [[A]] The semiconductor apparatus

as set forth in claim 2, wherein said delay monitor circuit comprises a control means for controlling a power source voltage ~~to be~~ supplied to said target circuit based on delay information generated by a delay element array formed in a time sharing ~~way~~ manner.

--4. (Currently Amended) [[A]] The semiconductor apparatus as set forth in claim 3, wherein said control circuit compares a plurality of delay ~~information~~ informations generated by a plurality of delay element arrays formed in the ~~above~~ delay means, judges a delay information with [[the]] a largest delay value as a final delay information and controls said power source voltage based on the final delay information.

--5. (Currently Amended) A semiconductor apparatus having a delay monitor circuit for ~~perceiving~~ monitoring critical path delay characteristics of a target circuit including a plurality of circuits operating at a plurality of different clock frequencies, wherein[[:]] said delay monitor circuit comprises:

[[a]] delay means having a plurality of delay elements for forming delay element arrays in accordance with supplied configuration information including a delay component to cause a signal propagation delay ~~inside~~ in said target circuit;

a plurality of registers ~~to be set~~ for setting therein a plurality of configuration ~~information~~ informations

for forming said delay element arrays in accordance with said plurality of different clock frequencies;

[[a]] first switching means for selectively switching the configuration information of said plurality of registers and supplying the configuration information to said delay means; and

[[a]] second switching means for selectively switching said plurality of ~~clocks and supplying~~ different clock frequencies for supply to said delay means.

--6. (Currently Amended) [[A]] The semiconductor apparatus as set forth in claim 5, wherein:

said first switching means switches the configuration information of delay element arrays set to a plurality of registers in a time sharing ~~way~~ manner and supplies the configuration information to said delay means; and

said second switching means switches said plurality of ~~clocks~~ different clock frequencies in a time sharing ~~way and supplies~~ manner for supply to said delay means.

--7. (Currently Amended) [[A]] The semiconductor apparatus as set forth in claim 6, wherein said delay monitor circuit comprises a control means for controlling a power source voltage for supplying to said target circuit based on delay information generated by a delay element array formed in a time

sharing ~~way~~ manner.

--8. (Currently Amended) [[A]] The semiconductor apparatus as set forth in claim 7, wherein said control circuit compares a plurality of delay ~~information~~ informations generated by a plurality of delay element arrays formed in said delay means, and controls said power source voltage based on a delay information with [[the]] a largest delay ratio with respect to a clock cycle in a plurality of clock frequency domains.

--9. (Currently Amended) [[A]] The semiconductor apparatus as set forth in claim 8, wherein said plurality of registers [[are]] have set therein a plurality of configuration ~~information~~ informations corresponding to the respective clock frequency domains.